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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NORRIS, JEREMY C	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/787,139	EN ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13,23-26,32,37,38,40-46,48-54 and 56-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13,23,25,26,48-53,56 and 63* is/are allowed.

6)☒ Claim(s) *24,32,37,38,40-42,54 and 57-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 32 is rejected under 35 U.S.C. 102(e) as being anticipated by US 6,217,987 B1 (Ono)

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Examiner notes the limitation that the upper-layer conductor circuit be built "by a build up process" is a process limitation in a device claim and thus is considered only to the extent to which said limitation impact the structure of the device. Furthermore, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)).

Additionally, Examiner notes that the terms "upper" and "lower" are dependent on a particular orientation of the device and are not intrinsic properties. Thus any direction could be considered to be "upper" or "lower" as long as a consistent scheme is utilized.

Ono discloses, a multilayer printed circuit board comprising a core board (1) having on both sides conductor circuits (4, 11) and, over each of said conductor circuits, buildup wiring layers comprising alternating an interlayer resin insulating layer (2) and a conductor layer (12, 13) thereon, wherein the conductor layers having a thickness of 10 to 30 μm (see col. 31, lines 10-20) are interconnected by via holes (6), wherein said core board comprises a plated-through hole (9) and a copper-clad laminate, each of said conductor circuit comprises a copper foil (8) of said copper-clad laminate and a plated metal layer (11), said conductor circuit on said core board is a conductor layer interconnected with said plated-through hole wherein the thickness of said conductor circuit (18 μm, see col. 29, lines 5-15) is not greater by more than 10μm than the thickness of said conductor layer (15 μm, see col. 31, lines 10-20) on said interlayer resin insulating layer [claim 32].

Claims 37, 38, 40-42, 44, 62, 66, and 67 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,214,445 B1 (Kanbe).

Kanbe discloses, referring primarily to figure 10, a multilayer printed circuit board comprising a core board (10) having on both sides conductor circuits (203c, 204c) and over each of said conductor circuits, a buildup wiring layer comprising alternating an interlayer resin insulating layer (221, 231) and a conductor layer (225, 235) thereon

wherein said conductor layers are interconnected by via holes (225v, 235v), wherein said core board is a copper-clad laminate (see col. 9, lines 55-60) and is provided with plated through holes (271) each of said plated through holes has a through hole piercing through said core board having been plated and filled with a filler (216), said conductor circuit comprise a copper foil of said copper-clad laminate and a plated film said via holes are formed immediately over said plated through holes so as to cover the whole opening of the through holes in said plated through holes and are interconnected with said plated through holes [claim 37], wherein the through holes have a diameter of not more than 200μm (col. 11, lines 1-5) [claim 38], wherein lower-layer via holes (31, 32) are disposed immediately over said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes [claim 40].

Similarly, Kanbe discloses, multilayer printed circuit board comprising a core board (10) and, on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer (221, 231) and a conductor layer (225, 235) thereon, wherein the conductor layers are interconnected by via holes (225v, 235v), wherein said core board is provided with plated-through holes (271), each of said plated- through holes has a through hole piercing through said core board, having been plated and filled with a filler (216), with the whole surfaces of said filler which are exposed from said plated-through holes being covered with said conductor layer provided with lower-layer via holes [claim 41].

Additionally Kanbe discloses, multilayer printed circuit board comprising a core board (10) and, on both sides thereof, buildup wiring layers comprising alternating an

interlayer resin insulating layer (221, 231) and a conductor layer (225, 235) thereon, wherein the conductor layers are interconnected by via holes (225v, 235v), wherein said core board is provided with plated-through holes (271), and lower-layer via holes are disposed to cover the whole opening of through holes of said plated-though holes, said plated-through holes being interconnected with said lower-layer via holes [claim 42], wherein said lower-layer via holes are filled with metal [claim 44], wherein upper-layer via holes are disposed immediately over said lower-layer via holes and interconnected with said lower-layer via holes [claim 66], wherein a plated film constituting said lower-layer via hole is connected with a plated film constituting said plated through hole [claim 67].

Also, Kanbe discloses, a multilayer printed circuit board comprising a core board (10) and, on both sides thereof, buildup wiring layers comprising alternating an interlayer resin insulating layer (221, 231) and a conductor layer thereon (225, 235), wherein the conductor layers are interconnected by via holes (225v, 235v), wherein said core board is provided with plated-though holes (271), each of said plated-through holes has a through hole piercing through said core board, having been plated and filled with a filler (216), with the whole surfaces of said filler which are exposed from said plated-through holes being covered with the conductor layers provided with lower-layer via holes, and said lower-layer via holes being interconnected with said plated-through holes via the conductor layer [claim 62].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,217,987 B1 (Ono) in view of US 6,132,853 (Noddin).

Ono discloses a printed circuit board comprising a substrate board (1) formed with a lower layer conductor circuit (4, 11) and built thereon an upper layer conductor circuit (12, 13) with an inter layer resin insulating layer (2) interposed in between, with said upper layer conductor circuit and said lower layer conductor circuit being interconnected by via holes (6), wherein said lower layer conductor circuit has a roughened surface (11) on a side which contacts with said interlayer resin insulating layer, said upper layer conductor circuit comprises an electroless plated film (12) and an electroplated film (13) said interlayer resin insulating layer is provided with a roughened surface, with said electroless plated film being complementary to said roughened surface, and said interlayer resin insulating layer and said via holes are provided with the same electroless plated film, with said electroless plated film formed on the bottoms of said via holes having a thickness equal to 50 to 100% of the thickness of said electroless plated film on said interlayer resin insulating layer and said lower-layer conductor circuit and said electroless plated film formed on the bottom of said via hole are connected through said roughened surface of said lower-layer conductor (see fig. 14). Ono does not specifically state that the via hole has a diameter of 80 μm or less [claim 24]. However, this range of via hole diameters is well known in the art as evidenced by Noddin (col. 3, lines 15-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the via hole in the invention of Ono with a diameter of 80 μm or less as is known in the art and evidenced by Noddin. The motivation for doing so would have been to use a via with sufficient size for signal transmission while not needlessly squandering board space. Moreover, it has

been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claims 40, 64, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe in view of US 5,243,142 (Ishikawa).

Kanbe discloses the claimed invention as described above including wherein lower-layer via holes are disposed immediately over said plated-through holes, said plated-through holes being interconnected with said lower-layer via holes. Kanbe does not specifically state that the filler comprises a metal particle [claim 40]. However, it is well known in the art to use fillers in plated through holes that comprise metal particles as evidenced by Ishikawa (col. 5, lines 25-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a filler containing metal particles in the invention of Kanbe as is known in the art and evidenced by Ishikawa. The motivation for doing so would have been to enhance the electrical connection. Additionally, the modified invention of Kanbe teaches that the metal particle is at least one selected from the group consisting of copper, gold, silver, aluminum, palladium and platinum (Ishikawa, col. 5, lines 25-45) [claim 64], wherein particle diameter of said metal particle is within the range of 0.1 to 50 μm (Ishikawa col. 5, lines 25-45) [claim 65]

Claims 43, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe in view of US 5,699,613 (Chong).

Kanbe discloses the claimed invention as described above except Kanbe does not specifically state bumps formed immediately above said plated-through holes [claim 43]. However, it is well known in the art to form bumps over plated through holes as evidenced by Chong (figure 9). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form bumps over the plated through holes in the invention of Kanbe as is known in the art and evidenced by Chong. The motivation for doing so would have been to allow for connection of the through hole to an integrated circuit device.

Also, regarding claims 45 and 46, Kanbe discloses the claimed invention as described above except Kanbe does not specifically state wherein valleys of said lower-layer via holes are filled with a conductive paste [claim 45], wherein valleys of said lower-layer via holes are filled with a resin [claim 46]. However, Chong teaches filling in valleys of via holes with a conductive resin paste (col. 4, lines 5-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to fill the via holes in the invention of Kanbe as taught by Chong. The motivation for doing so would have been to improve the structural integrity and electrically conductivity of the via holes.

Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ono in view of Noddin as applied to claim 24 above, and further in view of US 5,306,336 (Martyak).

The modified invention of Ono teaches the claimed invention as described above except modified Ono does not specifically teach that the electroless plating solution is formed from an electroless plating solution comprising tartaric acid or a salt thereof [claim 54]. However, it is well known in the art to use tartaric acid or slats thereof for electroless plating solutions as evidenced by Martyak (see col. 3, lines 20-45). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the solution taught by Martyak in the modified invention of Ono. The motivation for doing so would have been to easily manufacture the copper layer using a sulfate-free solution which is more environmentally friendly. Moreover, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Claims 58 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe in view of US 6,225,396 B1 (Watada).

Kanbe discloses the claimed invention as described above except Kanbe does not specifically state that the filler comprises SiO_2 beads having a maximum particle size of 15 μm [claims 58, 60]. However, it is well known in the art to form a filler with SiO_2 beads having a maximum particle size of 15 μm as evidenced by Watada (see col. 9,

lines 50-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the filler with SiO_2 beads having a maximum particle size of 15 μm in the invention of Kanbe as is known in the art and evidenced by Watada. The motivation for doing so would have been to make the device more resistant to failure due to heat (see Watada col. 3, lines 5-15).

Claims 59 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanbe in view of Ono.

Kanbe discloses the claimed invention as described above except Kanbe does not specifically state that the conductor circuit on said core board have a roughened layer on the surface [claims 59, 61]. However, it is well known in the art to form a roughened layer on the surface of conductor circuits as evidenced by Ono (see col. 8, lines 1-5). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form a roughened layer on the surface of the conductor circuits in the invention of Chong as is known in the art and evidenced by Ono. The motivation for doing so would have been to make the device more resistant to failure due to peeling.

Response to Arguments

Applicant's arguments filed 1 May 2006 have been fully considered but they are not persuasive.

Applicant's arguments with respect to claims 24, 37, 38, 40-42, 54, 55, and 58-62 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claim 32, Applicants allege, ""that the thickness of each of said conductor circuit is not greater by more than 10 μm than the thickness of said conductor layer on said interlayer resin insulating layer". However, as noted above, Ono discloses the thickness of the conductor circuit and the conductor layer to be 18 μm and 15 μm respectively, which clearly is a difference less than 10 μm.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCSN

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